**Op Codes for Sequence of Instructions**

Instruction sequence for Group 3 A1(1st roll i.e. group 5) is EFGHBDJICAKL

ALU OPCODE is this way

and = 0000

or = 0001

add = 0010

sub = 0110

slt = 0111

nor = 0xC

sll = 0x8

srl = 0x9

sra = 0xA

RegDst is ( LW => 0 rest all cases => 1)

Control Signal is like this => RegDst, ALUSrc, MemToReg, RegWrite, MemRead, MemWrite, Branch, ALUOP( 4 bits ) , Jump => so in total 12 bits.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Instruction ID Sequence | Instruction Name | Op Code | Control Signal | Control in decimal | Control in hex |
| E | and | 1 | 100100000000 | 2304 | 0x00000900 |
| F | andi | 2 | 010100000000 | 1280 | 0x00000500 |
| G | or | 3 | 100100000010 | 2306 | 0x00000902 |
| H | ori | 4 | 010100000010 | 1282 | 0x00000502 |
| B | sub | 5 | 100100001100 | 2316 | 0x0000090C |
| D | subi | 6 | 010100001100 | 1292 | 0x0000050C |
| J | sw | 7 | 010001000100 | 1092 | 0x00000444 |
| I | lw | 8 | 011110000100 | 1924 | 0x00000784 |
| C | addi | 9 | 010100000100 | 1284 | 0x00000504 |
| A | add | 10 (a) | 100100000100 | 2308 | 0x00000904 |
| K | beq | 11 (b) | 000000101100 | 44 | 0x0000002C |
| L | j | 12 (c) | 000000000001 | 1 | 0x00000001 |